AMENDMENTS TO THE SPECIFICATION

Please replace the first full paragraph on page 6 with the following:

As shown in Fig. 2~~1C~~, each of the ID recognition processors 6-1 to 6-5 has a recognition unit 6a for performing recognition processing for respective images obtained under a plurality of read optical conditions, an evaluation unit 6b for calculating an evaluation score representing a read likelihood ratio for each read optical condition on the basis of the recognition result of the recognition unit 6a, and a memory 6c for storing the recognition result and evaluation score.

Please replace the first full paragraph on page 15 with the following:

Figs. 4A and 4B show an ID recognition sorter system according to the second embodiment of the present invention. The same reference numerals as in Figs. 1A, 1B, and 2 denote the same parts. In the second embodiment, a plurality of wafer IDs are stamped on a semiconductor wafer 11. When a notch is positioned in the front direction, as shown in Fig. 5~~6~~, alphanumeric characters are stamped as a wafer ID 12a on the left of the upper surface of the semiconductor wafer 11. Further, alphanumeric characters and a two-dimensional code are stamped as wafer IDs 20b and 20c on a lower surface 21 of the semiconductor wafer 11, as shown in Fig. 6~~7~~.

Please replace the paragraph bridging pages 15 to 16 with the following:

An image sensing optical section 101b of the ID recognition sorter 101 shown in Fig. 4B is different from the image sensing optical section 1b shown in Fig. 1B in that the image sensing optical section 101b further comprises a lens 25 for condensing light reflected by the lower surface of a semiconductor wafer, a camera 26 for receiving

the image of the lower surface of the wafer via the lens 25 and outputting it to the ID recognition processors 6-6 to 6-10 and 6-11 to 6-15, and reflecting mirrors 22 for reflecting incident light from light sources 14 to the lower surface of the semiconductor wafer 11. The ID recognition processors 6-6 to 6-15 have the same arrangement as that of the ID recognition processors 6-1 to 6-5 shown in Fig. 2~~1C~~.